S/N 09/945,500 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner: Ly D. Pham
Serial No.:	09/945,500	Group Art Unit: 2827
Filed:	August 30, 2001	Docket: 1303.029US1
Title:	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS	

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Mail Stop 313 (c)
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Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date/Issue Date	Attorney Docket	Title
11/062543	February 22, 2005	1303.028US2	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
11/063825	February 23, 2005	1303.132US1	GERMANIUM-SILICON-CARBIDE FLOATING GATES IN MEMORIES

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicants request that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,
LEONARD FORBES

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Date 11 July '05 By
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I hereby certify that this paper is being transmitted by facsimile to the U.S. Patent and Trademark Office on the date shown below.

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July 11, 2005
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